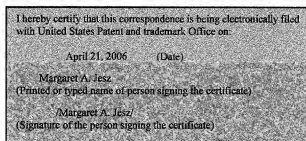


IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Theodore F. Vaida, *et al.*
Serial No.: 09/851,504
Filed: May 8, 2001
Title: A FIELD PROGRAMMABLE NETWORK APPLICATION SPECIFIC
INTEGRATED CIRCUIT AND A METHOD OF OPERATION
THEREOF
Grp./A.U.: 2663
Examiner: Due T. Duong

Sir:

STATEMENT OF THE SUBSTANCE OF APPLICANT INITIATED INTERVIEW IN
ACCORDANCE WITH C.F.R. § 1.133(b)

Summarized below is the substance of a telephone interview between Examiner Petranek and the under signed agent of record, held on April 20, 2006.

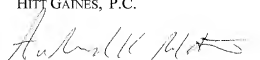
In the telephone interview, Examiner Duong and Mr. Ralston discussed distinctions between the claimed subject matter of the application and U.S. Patent No. 6,347,347 to Brown, *et al.* Specifically, the Examiner and Mr. Ralston discussed whether Brown teaches "a programmable logic core having an array of dynamically configurable arithmetic logic units" as claimed in independent

Claims 1, 11, 21 and 31. The Examiner reiterated his assertion that Brown teaches this limitation in FIG. 2 and column 4, lines 36-47. Mr. Ralston disputed this conclusion, noting that Brown does not teach an arithmetic logic unit (ALU) in any form, and that one of ordinary skill in the art would not find a teaching of an ALU in the cited portions of Brown.

The Applicants request the Examiner to telephone the undersigned agent of record at (972) 480-8800 if such would further or expedite the prosecution of the present application.

Respectfully submitted,

HITT GAINES, P.C.

A handwritten signature in dark ink, appearing to read "Andrew R. K. Ralston", written over a light blue horizontal line.

Andrew R. K. Ralston
Registration No. 55,560

Dated: April 21, 2006